MALLA REDDY ENGINEERING COLLEGE(AUTONOMOUS)

M.Tech I Year I Semester (MR14) Supplementary End Examinations, May, 2015

TIME TABLE

TIME : 10:00 AM TO 1:00 PM

BRANCH : ECE

Date & Day	DS&CE	EMBEDDED SYSTEMS	VLSI SYSTEM DESIGN
18-05-2015 Monday	VLSI TECHNOLOGY & DESIGN (44101)	--	--
19-05-2015 Tuesday	ADVANCED DATA COMMUNICATIONS (44103)	--	--
20-05-2015 Wednesday	DIGITAL SYSTEM DESIGN (44102)	DIGITAL SYSTEM DESIGN (44102)	DIGITAL SYSTEM DESIGN (44102)
21-05-2015 Thursday	MICRO CONTROLLERS FOR EMBEDDED SYSTEM DESIGN (44104)	--	--
22-05-2015 Friday	EMBEDDED SYSTEM DESIGN (441A3)	--	CPLD & FPGA ARCHITECTURES AND APPLICATIONS (441C1)
23-05-2015 Saturday	CMOS DIGITAL INTEGRATED CIRCUIT DESIGN (441B1)	--	--

NOTE: Any clashes / Omissions in this time-table may be brought to the notice of the undersigned immediately

Date: 08-05-2015

Chief Controller of Examinations

Copy to:

1) HOD (ECE) for information & necessary action.

2) PG Engg. Coordinator (College). 3) Controller of Examination for information & necessary action.

4) To be displayed in all Notice Boards. 5) To be read in PG Engg. Classes.