ACADEMIC REGULATIONS, COURSE STRUCTURE

AND DETAILED SYLLABUS
UNDER

CHOICE BASED CREDIT SYSTEM (CBCS)

Effective from the Academic Year 2015-16

M. Tech. Two Year Degree Course

(MR-15 Regulations)

in

EMBEDDED SYSTEMS (ES)

Department of Electronics & Communication Engineering

MALLA REDDY ENGINEERING COLLEGE (Autonomous)

(An Autonomous Institution approved by UGC and affiliated to JNTUH, Approved by AICTE & Accredited by NAAC with 'A' Grade and NBA & Recipient of World Bank Assistance under TEQIP Phase – II, S.C 1.1)

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MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

MR 15– ACADEMIC REGULATIONS (CBCS) FOR M. Tech. (REGULAR) DEGREE PROGRAMME

Applicable for the students of M. Tech. (Regular) programme from the Academic Year ***2015-16*** and onwards

The M. Tech. Degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the programme and who fulfill all the requirements for the award of the Degree.

INSTITUTION VISION

A Culture of excellence , the hallmark of MREC as world class education center to impart Technical Knowledge in an ambience of humanity, wisdom, intellect, creativity with ground breaking discovery, in order to nurture the students to become Globally competent committed professionals with high discipline, compassion and ethical values.

INSTITUTION MISSION

Commitment to progress in mining new knowledge by adopting cutting edge technology to promote academic growth by offering state of art Under graduate and Post graduate programmes based on well-versed perceptions of Global areas of specialization to serve the Nation with Advanced Technical knowledge.

DEPARTMENT VISION

With a vision to develop innovative, globally competent and quality electronic engineers by imparting state of art technology to foster a climate of high professionalism, ethical values, excellence and devotion.

DEPARTMENT MISSION

- To enrich the knowledge of students through quality and value based education.
- To organize various effective training programs in order to compete the advanced technology.
- To produce employable under graduates and post graduates.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO1: To provide the post graduate students with an advanced technical knowledge in the area of Embedded Systems, so as to make them to design, analyze and create the product relevant to the course.

PEO2: To train the PG students in the field of Embedded Systems and make themselves as Research & Development engineers, industry ready with a focus on effective communication skills, team working and multidisciplinary approach.

PEO3: To continue in inducing & Practicing professional ethics, honest practices to make them responsible towards the society collectively.

PROGRAMME OUTCOMES (POs)

PO1: PG students acquired specialized and in depth knowledge in the areas of Embedded Systems.

PO2: PG Students can demonstrate their ability in analyzing the complex and critical engineering problems in their field, apart from solving the subject problems.

PO3: PG Students can demonstrate their ability to think and work independently, with minimum or no supervision, and able to provide various solutions, by due considering the importance level of the technical requirement and associated issues.

PO4: PG Students can have the opportunity of working in Research & Development environment, in government organizations, and also able to develop intellectual property, patents etc.,

PO5: PG Students can have the opportunity to work in various industry standard tools like, Keil C Compilers , Flash Magic ,ARM and 80C51 Boards, Altera, MicroWind etc, which enables them industry ready, which in turn opens up and enhances the career opportunities.

PO6: PG Students can become, entrepreneurs, transforming their ideas into a product and systems to benefit the society, and empower themselves socially responsible.

PO7: PG Students are capable enough to write the technical reports, specifications and documenting the standards, which was imparted to them through training on communication skills, particularly verbal and written.

PO8: PG Students can work in multi cultural environment using their communication skills, and builds the interpersonal relationship in a team environment, capable of managing the team to achieve the goal of the project, and support the business and service motives of the organization.

PO9: PG Students can opt for higher education, particularly research in the field of Embedded Systems. Update the technical knowledge by involving in continuous learning process, being a member of profession body through research publications and in turn contribute back to the technical community.

PO10: Students can apply ethical and honest practices, to commit to the professional ethics expected from them and responsible towards the society.

PO11: Students can understand the impact of electronics products on to the global environmental perspective and demonstrate their skills and knowledge for sustained development.

1.0 ELIGIBILITY FOR ADMISSIONS :

Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.
Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the Government of Telangana or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.0 AWARD OF M.Tech. DEGREE :

2.1 A student shall be declared eligible for the award of the M.Tech. Degree, if the student pursues a course of study in not less than two and not more than four academic years. However, the student is permitted to write the examinations for two more years after four academic years of course work, failing which the student shall forfeit the seat in M. Tech. programme.

2.2 The student shall register for all 88 credits and secure all the 88 credits.

2.3 The minimum instruction days in each semester are 90.

3.0 COURSES OF STUDY :

The following specializations are offered at present for the M. Tech. programme of study.

1. Computer Science and Engineering
2. Digital Systems and Computer Electronics
3. Electrical Power Systems
4. Embedded Systems
5. Geotechnical Engineering
6. Machine Design
7. Structural Engineering
8. Thermal Engineering
9. VLSI System Design

and any other programme as approved by the University from time to time.

3.1 Departments offering M. Tech. Programmes with specializations are noted below:

CE	GTE	Geo Technical Engineering
	SE	Structural Engineering
EEE	EPS	Electrical Power Systems
ME	MD	Machine Design
	TE	Thermal Engineering
ECE	DSCE	Digital Systems and Computer Electronics
	ES	Embedded Systems
	VLSI SD	VLSI System Design
CSE	CSE	Computer Science and Engineering

4 COURSE REGISTRATION :

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work for the first semester through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'SUBSEQUENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'CURRENT SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from the Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.

4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Subject/ Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new Subject (subject to offering of such a Subject), or for another existing Subject (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5 ATTENDANCE :

The programmes are offered on a unit basis with each subject/course being considered as a unit.

5.1 Attendance in all classes (Lectures/Laboratories etc.) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the days of attendance in sports, games, NCC and NSS activities for appearing for the Semester End examination (SEE). A student shall not be permitted to appear for the Semester End Examinations (SEE) if his attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee (CAC).

5.3 Shortage of Attendance below 65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their end Semester End Examination of that subject and their registration shall stand cancelled.

5.5 A fee prescribed by the CAC, shall be payable towards Condonation of shortage of attendance.

5.6 A Candidate shall put in a minimum required attendance in atleast three (3) theory subjects in I semester for promoting to II Semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

5.7 A student shall not be promoted to the next semester unless the student satisfies the attendance requirement of the present Semester, as applicable. The student may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, the student shall not be eligible for readmission into the same class.

6 EVALUATION - DISTRIBUTION AND WEIGHTAGE OF MARKS: :

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Continuous Internal Evaluation and Semester End Examinations. For all Subjects/ Courses, the distribution shall be 40 marks for CIE, and 60 marks for the SEE

6.1 Theory Courses :

6.1.1 Continuous Internal Evaluation (CIE):

The CIE consists of two Assignments each of 05 marks and two mid-term examinations each of 35 marks. The CIE shall be finalized based on the 70% of the best performed and 30% of the other performance.The first mid-term examination shall be conducted for the first 50% of the syllabus, and the second mid-term examination shall be conducted for the remaining 50% of the syllabus.

First Assignment should be submitted before the conduct of the first mid-term examinations, and the Second Assignment should be submitted before the conduct of the second midterm examinations. The Assignments shall be as specified by the concerned subject teacher.. Each mid-term examination shall be conducted for a total duration of 120 minutes, for 35 marks.

The division of marks for CIE is as given below:

Mid – Term Examination				
Part	**Type of Questions**	**No. of questions**	**Marks per question**	**Total**
Part A	Multiple-choice questions	10	0.5	05
	Fill-in the blanks	10	0.5	05
	Sub-Total			10
Part B	Compulsory questions	5	2	10
Part C	Choice questions (3 out of 5)	3	5	15
			Mid-Term Exam Total	35
			Assignment	05
			Grand Total	40

6.1.2 Semester End Examination (SEE):

The division of marks for SEE is as given below:

Semester End Examination				
Part	**Type of Questions**	**No. of questions to be answered**	**Marks per question**	**Total**
Part A	Compulsory Questions (One from each module)	5	4	20
Part B	Choice Questions (5 out of 8) (Minimum one from each module)	5	8	40
			Grand Total	60

6.2 Practical Courses:

6.2.1 Continuous Internal Evaluation (CIE):

There will be CIE for 40 marks, shall be awarded with a distribution of 20 marks for day-to-day performance and timely submission of lab records, 5 marks for viva-voce, 15 marks for internal lab exam (best out of two exams).

6.2.2 Semester End Examination (SEE):

There will be SEE for 60 marks, shall be awarded with a distribution of 20 marks for write-up on the given experiment, 20 marks for proficiency in the exam, 10 marks for results and 10 marks for viva-voce. For conducting SEE, one internal examiner and one external examiner will be appointed by the Chief Controller of Examinations of the College. The external examiner should be selected from outside the College among the autonomous/reputed institutions, from a panel of three examiners submitted by the concerned Head of the Department.

6.3 Seminar:

There shall be two seminar presentations during I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 100 marks with a distribution of 30 marks for the report, 50 marks for presentation and 20 marks for the queries. A candidate has to secure a minimum of 50% of marks to be declared successful. If the student fails to fulfill minimum marks, the student has to reappear during the supplementary examinations.

6.4 Comprehensive Viva-Voce:

There shall be a Comprehensive Viva-Voce in III Semester. The Comprehensive Viva-Voce is intended to assess the students' understanding

of various subjects studied during the M. Tech. course of study. The Head of the Department shall be associated with the conduct of the Comprehensive Viva-Voce through a Committee. The Committee consists of the Head of the Department, one senior faculty member and an external examiner. The external examiner shall be appointed by the Chief Controller of Examinations from a panel of three examiners submitted by the concerned Head of the Department. There are no internal marks for the Comprehensive Viva-Voce and evaluates for maximum of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If the student fails to fulfill minimum marks, the student has to reappear during the supplementary examinations.

6.5. **General:** A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the Semester End Examination and a minimum of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together. In case the candidate does not secure the minimum academic requirement in any subject he has to reappear for the Semester End Examination in that subject. A candidate shall be given one chance to re-register for the subject if the internal marks secured by the candidate are less than 50% and failed in that subject. This is allowed for a maximum of three subjects and should register within two weeks of commencement of that semester class work. In such a case, the candidate must re-register for the subjects and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon the eligibility for writing the Semester End Examination in those subjects. In the event of the student taking another chance, the student's Continuous Internal Evaluation (CIE) marks and Semester End Examination (SEE) marks obtained in the previous attempt stands cancelled.

7 EXAMINATIONS AND ASSESSMENT - THE GRADING SYSTEM :

7.1 Marks will be awarded to indicate the performance of each student in each Theory Subject, or Lab / Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 6 above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	Grade Points	Letter Grade (UGC Guidelines)
≥ 80%	10	O (Outstanding)
≥ 70% to < 80%	9	A+ (Excellent)
≥ 60% to < 70%	8	A (Very Good)
≥ 55% to < 60%	7	B+ (Good)
≥ 50% to < 55%	6	B (Above Average)
< 50%	0	F (Fail)
Absent	Ab	Ab

7.3 A student obtaining F Grade in any Subject shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those Subjects will remain the same as those he obtained earlier.

7.4 A student not appeared for examination then 'Ab' Grade will be allocated in any Subject shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when conducted.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

7.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

7.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding 'Credit Points' (CP) is computed by multiplying the Grade Point with Credits for that particular Subject/ Course.
Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.8 The Student passes the Subject/ Course only when he gets GP ≥ 6(B Grade or above).

7.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (∑CP) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as:

$$\text{SGPA} = \left\{\sum_{i=1}^{N} C_i G_i\right\} / \left\{\sum_{i=1}^{N} C_i\right\} \ldots \text{For each Semester}$$

where 'i' is the Subject indicator index (takes into account all Subjects in a Semester), 'N'is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to the i^{th} Subject, and G represents the Grade Points (GP) corresponding to the Letter Grade awarded for that i^{th} Subject.

7.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the II Semester onwards, at the end of each Semester, as per the formula

$$\text{CGPA} = \left\{\sum_{j=1}^{M} C_j G_j\right\} / \left\{\sum_{j=1}^{M} C_j\right\} \ldots \text{for all S semesters registered}$$
(i.e., upto and inclusive of S semesters, S ≥ 2)

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' from the 1stSemester onwards upto and inclusive of the

Semester S (obviously M > N), 'j' is the Subject indicator index (takes into account all Subjects from 1 to S Semesters), C_j is the no. of Credits allotted to the j^{th} Subject, and G_j represents the Grade Points (GP)corresponding to the Letter Grade awarded for that j^{th} Subject. After registration and completion of I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

7.11 For Calculations listed in Item 7.6 – 7.10, performance in failed Subjects/ Courses (securing F Grade) will also be taken into account, and the Credits of such Subjects/Courses will also be included in the multiplications and summations.

8. EVALUATION OF PROJECT/DISSERTATION WORK :

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

8.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of 3 months between them.

8.6 The work on the project shall be initiated at the beginning of the III Semester and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.
Note: *The project supervisor/guide has to ensure that the student has to publish a minimum of one paper related to the thesis in a National/International Conference/Journal.*

8.7 For the final approval by the PRC, the soft copy of the thesis should be submitted for ANTI-PLAGIARISM for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than 24%, then only thesis will be accepted for submission.

8.8 Three copies of the Project Thesis certified by the supervisor, HOD and Principal shall be submitted to the Chief Controller of Examinations for project evaluation (viva voce).

8.9 For Project work part-I in III Semester there is an internal marks of 50, the evaluation should be done by the PRC for 30 marks and Supervisor will evaluate for 20 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain. A candidate has to secure a minimum of 50% of marks to be declared successful for Project work part-I. If the student fails to fulfill minimum marks, the student has to reappear during the supplementary examination.

8.10 For Project work part-II in IV Semester there is an internal marks of 50, the evaluation should be done by the PRC for 30 marks and Supervisor will evaluate for 20 marks. The PRC will examine the overall progress of the Project Work and decide the Project is eligible for final submission or not. A candidate has to secure a minimum of 50% of marks to be declared successful for Project work part-II. If the student fails to fulfill minimum marks, the student has to reappear during the supplementary examination.

8.11 For Project Evaluation (Viva Voce) in IV Semester there is an external marks of 150 and the same evaluated by the External examiner appointed by the Chief Controller of Examinations. For this, the Head of the Department shall submit a panel of 3 examiners, eminent in that field, with the help of the supervisor/guide concerned. The candidate has to secure minimum of 50% marks in Project Evaluation (Viva-Voce) examination.

8.12 If the student fails to fulfill as specified in 8.11, based the recommendation of the external examiner, the student will reappear for the Viva-Voce examination with the revised thesis only after three months. In the reappeared examination also, fails to fulfill, the student will not be eligible for the award of the degree.

8.13 The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva-Voce examination.

9. AWARD OF DEGREE AND CLASS :

9.1 A Student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of **88** Credits (with CGPA $\geq$ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

9.2 Award of Class

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	≥ 6.75 and < 7.75
Second Class	≥ 6.00 and < 6.75

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10. WITHHOLDING OF RESULTS :

If the student has not paid the dues, if any, to the University or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

11. TRANSITORY REGULATIONS :

11.1 If any candidate is detained due to shortage of attendance in one or more subjects, they are eligible for re-registration to maximum of three earlier or equivalent subjects at a time as and when offered.

11.2 The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per MR15 Academic Regulations.

12. GENERAL :

12.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

12.2 **Credit Point:** It is the product of grade point and number of credits for a course.

12.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”.

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the CAC is final.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the SEE)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to that course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester. The Hall Ticket of the candidate shall be cancelled.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including practicals and project

		work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all SEE. The continuation of the programme by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all SEE. The continuation of the programme by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course.
6	Refuses to obey the orders of the Chief Controller of Examinations (CCE) / Controller of Examinations (CE) / Assistant Controller of Examinations (ACE) / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a

	the officer in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination	police cases registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all SEE. The continuation of the programme by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred and forfeits the seat.

		Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that course and all other courses the candidate has appeared including practical examinations and project work of that SEE.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the CCE for further action toward suitable punishment.	

Note: ***The student(s) found indulging in malpractices during the CIE also will be punished based on the recommendations of the College Academic Committee.***

MALLA REDDY ENGINEERING COLLEGE (Autonomous)

Academic Year 2015-16 (Choice Based Credit System)

COURSE STRUCTURE – M.TECH Embedded Systems (ES)

(MR15 Regulations)

I SEMESTER

S. No.	Category	Course Code	Name of the course	Contact hours/ week			Credits	Scheme of Valuation		Total Marks
				L	T	P		Internal (CIE)	External (SEE)	
1	CC I	54106	Embedded System Design	4	--	--	4	40	60	100
2	CC II	54301	ARM Architectures	4	--	--	4	40	60	100
3	CC III	54116	Real Time Operating Systems	4	--	--	4	40	60	100
4	PE I	55134	Advanced Computer Architecture	4	--	--	4	40	60	100
		54101	VLSI Technology and Design							
		54302	Embedded Computing							
5	PE II	54102	Digital System Design	4	--	--	4	40	60	100
		54303	Embedded C							
		54121	Design for Testability							
6	PE III	54304	TCP/IP Networks	4	--	--	4	40	60	100
		54110	Coding Theory and Techniques							
		54111	Soft Computing Techniques							
7	Laboratory I	54126	Embedded System Lab	--	--	4	2	40	60	100
8	Seminar I	54305	Seminar - I	--	--	4	2	100	--	100
			Total	24	--	8	28	Contact Periods: 32		

II SEMESTER

S. No.	Category	Course Code	Name of the course	Contact hours/ week			Credits	Scheme of Valuation		Total Marks
				L	T	P		Internal (CIE)	External (SEE)	
1	CC IV	54115	Digital Signal Processors and Architectures	4	--	--	4	40	60	100
2	CC V	54306	Embedded Networking	4	--	--	4	40	60	100
3	CC VI	54307	Sensors and Actuators	4	--	--	4	40	60	100
4	PE IV	54117	CPLD and FPGA Architectures and Applications	4	--	--	4	40	60	100
		54308	Wireless Communications and Networks							
		54119	System on Chip Architecture							
5	PE V	54309	Multimedia and Signal Coding	4	--	--	4	40	60	100
		54118	Network Security and Cryptography							
		54104	Hardware and Software Co-Design							
6	PE VI	54125	Scripting Languages	4	--	--	4	40	60	100
		54124	Ad hoc Wireless Networks							
		54122	Device Modeling							
7	Laboratory II	54310	Advanced Embedded System Lab	--	--	4	2	40	60	100
8	Seminar II	54311	Seminar - II	--	--	4	2	100	--	100
Total				24	--	8	28	Contact Periods: 32		

III Semester

S. No.	Category	Course Code	Name of the course	Contact hours/ week			Credits	Scheme of Valuation		Total Marks
				L	T	P		Internal (CIE)	External (SEE)	
1	CV	54312	Comprehensive Viva-Voce	--	--	--	4	--	100	100
2	PR I	54313	Project work Part I	--	--	16	8	50	--	50
Total				--	--	16	12	Contact Periods: 16		

IV Semester

S. No.	Category	Course Code	Name of the course	Contact hours/week			Credits	Scheme of Valuation		Total Marks
				L	T	P		Internal (CIE)	External (SEE)	
1	PR II	54314	Project work Part II	--	--	16	8	50	--	50
2	PR III	54315	Project Viva-Voce	--	--	--	12	--	150	150
Total				--	--	16	20	Contact Periods: 16		

*** CC – Core Course, PE – Professional Elective, CV – Comprehensive Viva – Voce, PR – Project Work**

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Course Code: 54106 **Credits: 4**

M.Tech. – I Semester

EMBEDDED SYSTEM DESIGN

PREREQUISITES: Microprocessors and Microcontrollers.

OBJECTIVE: This course introduces the difference between Embedded Systems and General purpose systems. This course familiarize to compare different approaches in optimizing General purpose processors. This course provides the design tradeoffs made by different models of embedded systems.

Module - I: Introduction to Embedded Systems [8 Periods]
Definition of Embedded System, Embedded Systems Vs General Computing Systems, History ofEmbedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

Module - II: Typical Embedded System [12 Periods]
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

Module - III: Embedded Firmware [10 Periods]
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

Module - IV: RTOS Based Embedded System Design [12 Periods]
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

Module - V: Task Communication [8 Periods]
Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Shibu K.V, **Introduction to Embedded Systems**, McGraw Hill.(Module – I, II, III, IV, V)

REFERENCE BOOKS:
1. Raj Kamal , **Embedded Systems**,TMH.
2. Frank Vahid, Tony Givargis, John Wiley, **Embedded System Design**.
3. Lyla **, Embedded Systems**, Pearson, 2013
4. David E. Simon, **An Embedded Software Primer** , Pearson Education.

COURSE OUTCOMES:

At the end of the course students are able to:

1. Understand the basics of an embedded system.
2. Design, implement and test an embedded system.
3. Understand the design tradeoffs made by different models of embedded systems.

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Course Code: 54301 **Credits: 4**

M.Tech. – I Semester

ARM ARCHITECTURES

PREREQUISITES: CISC and RISC Architecture and Assemble Language, Embedded C

OBJECTIVE: To know about ARM Processor Registers, Instruction pipeline, Interrupts and Architecture, to learn about Instructions, Addressing modes and conditional instructions, to learn about Cache architecture, Polices, Flushing, MMU, page tables, translational, and access permissions.

Module - I: ARM ARCHITECTURE [7 Periods]

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

Module - II: ARM PROGRAMMING MODEL – I [8 Periods]

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

Module - III: ARM PROGRAMMING MODEL – II [9 Periods]

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

Module - IV: ARM PROGRAMMING [9 Periods]

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

Module - V: MEMORY MANAGEMENT [8 Periods]

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. Andrew N.Sloss, Dominic Symes, Chris Wright, **ARM Systems Developer's Guides-Designing & Optimizing System Software**, Elsevier, 2008.

REFERENCE BOOKS:

1. Jonathan W. Valvano – Brookes/ Cole, **Embedded Microcomputer Systems, Real Time Interfacing**, Thomas Learning, 1999.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Know about ARM Processor Registers, Instruction pipeline, Interrupts and Architecture
2. Learn about Instructions, Addressing modes and conditional instructions.
3. Learn about Cache architecture, Polices, Flushing, MMU, page tables, translational, and access permissions.

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Course Code: 54116 **Credits: 4**

M.Tech. – I Semester

REAL TIME OPERATING SYSTEMS

PREREQUISITES: Embedded System Concepts and Linux and UNIX Programming

OBJECTIVE: To learn fundamentals of UNIX operating system. To study implementation aspects of real time concepts. To study example RTOSs and applications.

Module - I: Introduction **[8 Periods]**
Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec.

Module - II: Real Time Operating Systems **[9 Periods]**
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

Module - III: Objects, Services and I/O **[7 Periods]**
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/OConcepts, I/O Subsystem

Module - IV: Exceptions, Interrupts and Timers **[8 Periods]**
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

Module - V: Case Studies of RTOS **[9 Periods]**
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS and Basic Concepts of Android OS.

TEXT BOOKS:
1. Qing Li, **Real Time Concepts for Embedded Systems**, Elsevier, 2011

REFERENCE BOOKS:
1. Rajkamal, **Embedded Systems- Architecture, Programming and Design,**TMH, 2007,.
2. Richard Stevens, **Advanced UNIX Programming**,
3. Dr. Craig Hollabaugh , **Embedded Linux: Hardware, Software and Interfacing**

COURSE OUTCOMES:
After completion of the course, students will be able to:

1. Understand the fundamentals of UNIX operating system.
2. Understand the implementation aspects of real time concepts.
3. Understand the example RTOSs and applications.

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Course Code: 55134 **Credits: 4**

M.Tech. – I Semester

ADVANCED COMPUTER ARCHITECTURE

(Professional Elective – I)

PREREQUISITES: Computer Networks and Computer Architecture.

OBJECTIVE: To emphasize on the concept of a complete system consisting of asynchronous interactions between concurrently executing hardware components and device driver software in order to illustrate the behavior of a computer system as a whole, To understand the advanced concepts of computer architecture and exposing the major differentials of RISC and CISC architectural characteristics.

Module - I: Fundamentals of Computer Design [10 Periods]

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

Module - II: Pipelines [8 Periods]

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. **Memory Hierarchy Design:** Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

Module - III: Instruction Level Parallelism (IlP) - The Hardware Approach [10 Periods]

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation. **ILP Software Approach:** Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

Module - IV: Multi Processors and Thread Level Parallelism [7 Periods]

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

Module - V: Inter Connection and Networks [8 Periods]

Introductions, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, **Computer Architecture: A Quantitative Approach**, an Imprint of Elsevier, 3rd Edition.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti **-, Modern Processor Design : Fundamentals of Super Scalar Processors**
2. Kai Hwang, Faye A.Brigs, Computer **Architecture and Parallel Processing** , MC Graw Hill.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Understand the advanced concepts of computer architecture and exposing the major differentials of RISC and CISC architectural characteristics.
2. Investigating modern design structures of Pipelined and Multiprocessors systems.
3. Become acquainted with recent computer architectures and I/O devices, as well as the low-level language required to drive/manage these types of advanced hardware.

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Course Code: 54101

Credits: 4

M.Tech. – I Semester

VLSI TECHNOLOGY AND DESIGN

(Professional Elective – I)

PREREQUISITES: STLD and IC Technology

OBJECTIVE: To Understand the VLSI technology and design of circuits based on technology like cmos, bicmos etc, to Understand the designing layouts of logic gates, to understanding the combinational logic networks and its optimization , to understanding the sequential systems and its optimization, to get knowledge on floor plan design

Module –I **[10 Periods]**

Crystal Growth and Wafer Preparation: Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Process Considerations.

Epitaxy: Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation.

Oxidation : Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopant At interface, Oxidation of Poly Silicon, Oxidation inducted Defects

Module –II **[9 Periods]**

Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography.

Reactive Plasma Etching: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes.

Module –III **[8 Periods]**

Dielectric and Polysilicon Film Deposition: Introduction, Deposition Processes, Polysilicon, Silicon Dioxide, Silicon Nitride, Plasma Assisted Depositions, Other Materials.

Diffusion: Models of Diffusion in Solids, Flick's one Dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques

Module -IV **[9 Periods]**

Ion Implantation: Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation.

Metallization: Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization Problems..

Module -V **[8 Periods]**
MOS Technology: NMOS, PMOS, CMOS, BICMOS, Latch up,

Basic Electrical Properties of MOS and BICMOS circuits : I_{ds}-V_{ds} relationships, MOS transistor threshold Voltage(Vt), Pass transistor, NMOS Inverter, Determination of pull-up to pull-down ratios, Various pull ups of MOS and BICMOS inverter, Lambda based Design Rules

Text Books:
1. S. M. Sze, "**VLSI Technology**", McGraw-Hill, Second Edition,2003, TMH NewDelhi.
2. Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, **Essentials of VLSI circuits and systems** –2005, PHI New Delhi.

Reference Books:
1. S.K. Ghandhi, "**VLSI Fabrication Principles**", John Wiley Inc., Second Edition New York, 1994.

COURSE OUTCOMES:
After completion of the course, students will be able to:

1. Student will be in a position that he/she can design vlsi circuits starting from pmos nmos, cmos, and bicmos technology based design
2. Gains thorough knowledge on design tools to draw layouts for the transistor structures
3. The student will understand the design of logic gates
4. The student will understand the design of sequential systems

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Course Code: 54302 **Credits: 4**

M.Tech. – I Semester

EMBEDDED COMPUTING

(Professional Elective – I)

PREREQUISITES: Embedded Systems and Implementation and also requires Concepts of LINUX **.**

OBJECTIVE: To learn about System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System and Busy Box, To know about Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls and network security, To learn about IA32 Instruction Set, application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools

Module - I: PROGRAMMING ON LINUX PLATFORM [8 Periods]

System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box.
Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

Module –II: INTRODUCTION TO SOFTWARE DEVELOPMENT TOOLS[9 Periods]

GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,.

Module - III: INTERFACING MODULES [8 Periods]

Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, Open CV for machine vision, Audio signal processing.

Module - IV: NETWORKING BASICS [8 Periods]

Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

Module - V: IA32 INSTRUCTION SET [9 Periods]

Application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:

1. Peter Barry and Patrick Crowley, **Modern Embedded Computing**,Elsevier/Morgan Kaufmann ,1stEd,2012.
2. Michael K. Johnson, Erik W. Troan, **Linux Application Development,** Adission Wesley, 1998.
3. Kip R. Irvine, **Assembly Language for x86 Processors**

4. Intel® 64 and IA-32 **Architectures Software Developer Manuals**

REFERENCE BOOKS:

1. Abraham Silberschatz, Peter B. Galvin and Greg Gagne, **Operating System Concepts**.
2. Maurice J. Bach Prentice, **The Design of the UNIX Operating System,** Hall.
3. W. Richard Stevens, **UNIX Network Programming.**

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Learn about System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System and Busy Box
2. Know about Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls and network security.
3. Learn about IA32 Instruction Set,application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools

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Course Code: 54102 **Credits: 4**

M.Tech. – I Semester

DIGITAL SYSTEM DESIGN

(Professional Elective – II)

PREREQUISITES: VLSI and STLD

OBJECTIVE: To impart knowledge on the theory of Sequential machines and minimization of it. to design digital circuits for various applications. to learn fault diagnosis and testability algorithms.

MODULE – I :Minimization And Transformation Of Sequential Machines [8 Periods]

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.
Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

MODULE – II : Digital Design [9 Periods]

Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

MODULE – III : SM Charts [7 Periods]

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

MODULE – IV: Fault Modeling & Test Pattern Generation [8 Periods]

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

MODULE – V: Fault Diagnosis In Sequential Circuits [7 Periods]

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Charles H. Roth, **Fundamentals of Logic Design** ,Cengage Learning,5th Ed.
2. MironAbramovici, Melvin A. Breuer and Arthur D. Friedman **, Digital Systems Testing and Testable Design**, John Wiley & Sons Inc.
3. N. N. Biswas ,**Logic Design Theory** , PHI.

REFERENCE BOOKS:

1. Z. Kohavi ,**Switching and Finite Automata Theory**, TMH, 2nd Ed,2001.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Design digital circuits by their own for new applications.
2. Identify techniques to improve fault diagnosis for digital circuits.

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Course Code: 54303 **Credits: 4**

M.Tech. – I Semester

EMBEDDED C

(Professional Elective – II)

PREREQUISITES: C Language and Embedded System Concepts

OBJECTIVE: Understand the significance of programming embedded C in real time applications and to use it for specific applications, to gain knowledge on 8051 micro controller, to develop code for real time embedded world, to understand design of real time timers with various constraints, to understand and gain knowledge on Intruder Alarm System.

UNIT – I: PROGRAMMING EMBEDDED SYSTEMS IN C [9 Periods]

Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family: Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements , Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT – II: READING SWITCHES [8 Periods]

Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs(basic code), Example: Counting goats, Conclusions

UNIT – III: ADDING STRUCTURE TO THE CODE [7 Periods]

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV: MEETING REAL-TIME CONSTRAINTS [10 Periods]

Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V: CASE STUDY: INTRUDER ALARM SYSTEM [9 Periods]

Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Michael J. Pont, **Embedded C**, Pearson Education, 2nd Ed,2008.

REFERENCE BOOKS:

1. Nigel Gardner, **PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C**

COURSE OUTCOMES:

1. Able to understand the importance embedded C in so many applications like application specific micro controllers
2. Able to develop the quality based embedded systems like Intruder Alarm System
3. Able to understand the basic working modes of timers and its formatted data frames, its control.

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Course Code: 54121 **Credits: 4**

M.Tech. –I Semester

DESIGN FOR TESTABILITY

(Professional Elective - II)

PREREQUISITES: Digital Electronics, Digital signal Processing and VLSI Technology**.**

OBJECTIVE: To gain knowledge on digital testing as applied to VLSI design, to acquire knowledge on testing of algorithms for digital circuits, to learn various testing methods for digital circuits.

MODULE-I: Introduction to Testing **[12 Periods]**

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

MODULE -II: Logic And Fault Simulation **[12 Periods]**

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

MODULE-III: Testability Measures **[12 Periods]**

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

MODULE-IV: Built-In Self-Test **[12 Periods]**

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

MODULE-V: Boundary Scan Standard **[12 Periods]**

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. M.L. Bushnell, V. D. Agrawal, **"Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits",** Kluwer Academic Pulishers. 2004. (Modules I,II,III,IV & V)

REFERENCE BOOKS:

1. M. Abramovici, M.A.Breuer and A.D Friedman, **"Digital Systems and Testable Design"**, Jaico Publishing House.
2. P.K. Lala, **"Digital Circuits Testing and Testability"**, Academic Press.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Design complex digital systems using VLSI design methodology.
2. Design a digital system using given specifications and design constraints.
3. Assess logic and technology-septic parameters to control the functionality, system synchronization, power consumption, and Effects of circuit parasitic.

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Course Code: 54304 **Credits: 4**

M.Tech. – I Semester

TCP/IP NETWORKS

(Professional Elective –III)

PREREQUISITES: OSI/ISO Protocol and Network Protocols

OBJECTIVE: To Introduce the Concepts of TCP/IP Protocol and it's Layers

Module - I: Network Models **[8 Periods]**

Layered Tasks, The OSI Model, Layers in OSI Model, TCP/IP, Protocol suite, Addressing.

Network Layer Protocols: Internet Protocol (IP), ICMPv4, Mobile IP, IPv6, Addressing IPv6 Protocol, ICMPV6 Protocol, Transition from IPV4 to IPV6

Module - II: Transport Layer **[10 Periods]**

Introduction to Transport Layer, Transport Layer Protocols: Simple Protocols, Stop and Wait Protocols, Go Back N Protocol, Selective Repeat Protocol, Bidirectional Protocols: Piggybacking Transport layer protocols Services and Port Numbers.

Transmission Control Protocol: TCP Services, TCP Features, Segments, TCP Connection, State Transition Diagram, Windows in TCP, Flow and Error Control, TCP Congestion Control, TCP Timers.

Module - III: User Datagram Protocol **[8 Periods]**

User Datagram, UDP Services, UDP Applications.

Stream Control Transmission Protocol (SCTP): Services, Features, Packet Format, Flow Control, Error Control, Congestion Control.

Module - IV: Mobile Network Layer **[9 Periods]**

Entities and Terminology, IP Packet Delivery, Agents, Addressing, Agent Discovery, Registration, Tunneling and Encapsulating, Inefficiency in Mobile IP.

TCP in Wireless Domain: Traditional TCP, TCP Over Wireless, Snooping TCP, TCP Unware Link Layer. Indirect TCP, Mobile TCP, Explicit Loss Notification, WTCP, Transaction-Oriented TCP, Impact of Mobility.

Module - V: Congestion Control and Quality of Service **[8 Periods]**

Data Traffic, Congestion, Congestion Control, Qualityof Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks.

Queue Management: Passive-Drop trial, Drop front, Random drop, Active- early Random drop,Random Early detection

TEXT BOOKS:

1. MahbubHasan& Raj Jain, **High performance TCP/IP Networking** ,PHI ,2005.
2. B.A. Forouzan, **Data communication & Networking,**TMH, 5th Edition.

REFERENCES:

1. Douglas. E.Comer, **Internetworking with TCP/IP**, Volume I PHI.
2. Larry L. Perterson and Bruce S.Davie**, Computer Networks.**
3. JochenSchiiler, **Mobile Communications**, Pearson, Second Edition .

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Understand the concepts of Different Networks
2. Demonstrate the TCP/IP Layers and its Protocols

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Course Code: 54110 **Credits: 4**

M.Tech. – I Semester

CODING THEORY AND TECHNIQUES

(Professional Elective –III)

PREREQUISITES: Coding Techniques

OBJECTIVE: To know about the Information theory and source coding techniques. to learn concepts of channel coding techniques.

Module - I: Source Coding **[10 Periods]**

Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, coding for discrete less sources, Source coding theorem, fixed length and variable length coding, properties of prefix codes, Shannon-Fano coding, Huffman code, Huffman code applied for pair of symbols, efficiency calculations, Lempel-Ziv codes.

Module - II: Linear Block Codes **[8 Periods]**

Introduction to Linear block codes, Generator Matrix, Systematic Linear Block codes, Encoder Implementation of Linear Block Codes, Parity Check Matrix, Syndrome testing, Error Detecting and correcting capability of Linear Block codes. Hamming Codes, Probability of an undetected error for linear codes over a Binary Symmetric Channel, Weight Enumerators and Mac-Williams identities, Perfect codes, Application of Block codes for error control in data storage Systems.

Module - III: Cyclic Codes **[9 Periods]**

Algebraic structure of cyclic codes, Binary Cyclic code properties, Encoding in systematic and non-systematic form, Encoder using (n-k) bit shift register, Syndrome Computation and Error detection, Decoding of Cyclic Codes.

Module - IV: Convolution Codes **[10 Periods]**

Encoding of Convolution codes, Structural properties of Convolutional codes, state diagram, Tree diagram, Trellis Diagram, maximum, Likelihood decoding of Convolutional codes.Viterbi Algorithm, Fano, Stack Sequential decoding algorithms, Application of Viterbi and sequential decoding.

Module - V: BCH Codes **[11 Periods]**

Groups, fields, binary Fields arithmetic, construction of Falois fields GF (2m), Basic properties of Falois Fields, Computation using Falois Field GF (2m) arithmetic, Description of BCH codes, Decoding procedure for BCH codes.

TEXT BOOKS:

1. SHU LIN and Daniel J. Costello, **Error Control Coding – Fundamentals and Applications**, Jr. Prentice Hall Inc.
2. Fundamental and Application by Bernard Sklar , **Digital Communications** , Pearson Education Asia.

3. Man Young Rhee, **Error Control Coding Theory**, Mc. Graw Hill Publ.

REFERENCE BOOKS:

1. John G. Proakis, **Digital Communications**, Mc. Graw Hill Publication.
2. K. Sam Shanmugam, **Digital and Analog Communication Systems**.
3. Symon Haykin , **Digital Communications**.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Know about the Information, Entropy, Sourse coding techniques such as Shannon-Fano, Huffman ,Lempel Ziv coding techniques.
2. Understand channel coding techniques such as block code ,cyclic code, convolution codes and BCH codes.

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Course Code: 54111 **Credits: 4**

M.Tech. – I Semester

SOFT COMPUTING TECHNIQUES

(Professional Elective -III)

PREREQUISITES: Neural Networks and Fuzzy Logic Systems.

OBJECTIVE: To know about Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule based systems, To know about Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perception, Adeline and Madeline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, To learn about fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling

Module – I: Introduction **[10 Periods]**

Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rulebased systems, the AI approach, Knowledge representation - Expert systems.

Module - II: Artificial Neural Networks **[9 Periods]**

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

Module - III: Fuzzy Logic System **[8 Periods]**

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning,Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Selforganizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

Module - IV : Genetic Algorithm **[10 Periods]**

Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters,Solution of typical control problems using genetic algorithm, Concept on some other searchtechniques like Tabu search and anD-colony search techniques for solving optimization problems.

Module - V: Applications **[11 Periods]**

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:

1. Jacek.M.Zurada , **Introduction to Artificial Neural Systems**, Jaico Publishing House, 1999.
2. Kosko, B., Prentice, **Neural Networks and Fuzzy Systems**, Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:

1. Klir G.J. & Folger T.A, **Fuzzy Sets, Uncertainty and Information**, Prentice-Hall of India Pvt.Ltd, 1993.
2. Zimmerman H.J, **Fuzzy Set Theory and Its Applications**, Kluwer Academic Publishers, 1994.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Know about Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule based systems.
2. Know about Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perception, Adeline and Madeline, Feed-forward Multilayer Perceptron, Learning and Training the neural network.
3. Learn about fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling

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Course Code: 54126 **Credits: 2**

M.Tech. – I Semester

EMBEDDED SYSTEM LAB

Note: The following programs are to be implement on 89C51 Development board using Embedded C Language on Keil IDE and Flash magic.

List of experiments:

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions
11. Program to interfacing RFID.
12. Implementation of Traffic light controller.

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Course Code: 54305 **Credits: 2**

M.Tech. – I Semester

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Course Code: 54115 **Credits: 4**

M.Tech. – II Semester

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

PREREQUISITES: Signal Processing and Embedded Systems

OBJECTIVE: To impart the knowledge of basic DSP filters and number systems to be used, different types of A/D, D/A conversion errors. to gain concepts of digital signal processing techniques, implementation of DSP & FFT algorithms and also to learn about Interfacing of serial & parallel communication devices to the processor.

Module - I: Introduction to Digital Signal Processing [10 Periods]
Introduction, to a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation. **Computational Accuracy in DSP Implementations:** Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Module -II: Architectures for Programmable DSP Devices [8 Periods]
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Module - III: Programmable Digital Signal Processors [9 Periods]
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XXProcessors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

Module - IV: Analog Devices Family of DSP Devices [10 Periods]
Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.
Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

Module - V: Interfacing Memory And I/O Peripherals To Programmable DSP Devices [8 Periods]
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan **Digital Signal Processing** , Thomson Publications, 2004.
2. K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, **A Practical Approach to Digital Signal Processing**, New Age International, 2006/2009.

3. Woon-Seng Gan, Sen M. Kuo, **Embedded Signal Processing with the Micro Signal Architecture,**Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. B. Venkataramani and M. Bhaskar, **Digital Signal Processors, Architecture, Programming and Applications**, TMH, 2002.
2. Jonatham Stein , **Digital Signal Processing** , John Wiley, 2005.
3. Lapsley et al **, DSP Processor Fundamentals, Architectures & Features,** S. Chand & Co,2000.
4. The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar **, Digital Signal Processing Applications Using the ADSP-2100 Family** , PHI.
5. Steven W. Smith, Ph.D, California, **The Scientist and Engineer's Guide to Digital Signal Processing by Technical Publishing**, ISBN 0-9660176-3-3, 1997.
6. David J. Katz and Rick Gentile of Analog Devices, Newnes, **Embedded Media Processing**, ISBN 0750679123, 2005.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Comprehends the knowledge & concepts of digital signal processing techniques, basic building blocks, and implementation of DSP & FFT Algorithms.
2. Do Programming the DSP TMS320C54XX PROCESSOR and decimation interpolation filters, adaptive filters.
3. Learn about interfacing of serial & parallel communication devices to the processor.

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Course Code: 54306 **Credits: 4**

M.Tech. – II Semester

EMBEDDED NETWORKING

PREREQUISITES: Embedded Systems and Networks

OBJECTIVE: To understand the significance of embedded networks in real time applications and to use it for specific applications, to Know different types of communication protocols like serial and parallel communication protocols, to know different types of communication protocols which have embedded end modules, to understand wired and wireless communication protocols, its formats ,to understand and gain knowledge on wireless sensors and its application in wireless embedded networks

Module - I: Embedded Communication Protocols [8 Periods]

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols –Firewire.

Module - II: USB and CAN Bus [10 Periods]

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing –PIC microcontroller CAN Interface –A simple application with CAN.

Module - III: Ethernet Basics [9 Periods]

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

Module - IV: Embedded Ethernet [8 Periods]

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

Module - V: Wireless Embedded Networking [8 Periods]

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing –Data Centric routing.

TEXT BOOKS:

1. Frank Vahid, TonyGivargis, **Embedded Systems Design: A Unified Hardware/Software Introduction,** John & Wiley Publications, 2002
2. Jan Axelson, **Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port,** Penram Publications, 1996.

REFERENCE BOOKS:

1. Dogan Ibrahim, **Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series** ,Elsevier 2008.
2. Jan Axelson,**Embedded Ethernet and Internet Complete,** Penram publications, 2003.
3. Bhaskar Krishnamachari, **Networking Wireless Sensors,**Cambridge press 2005.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Understand the basic working modes of networks and its formatted data frames, its control
2. Understand the significance of embedded networks in real time applications and to use it for specific applications.
3. Know different types of communication protocols like serial and parallel communication protocols
4. Know different types of communication protocols which have embedded end modules
5. Understand wired and wireless communication protocols, its formats
6. Understand and gain knowledge on wireless sensors and its application in wireless embedded networks

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Course Code: 54307 **Credits: 4**

M.Tech. – II Semester

SENSORS AND ACTUATORS

PREREQUISITES: Embedded Systems Sensors and Sensor, Actuators Types.

OBJECTIVE: To learn about sensor Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), and Characterization, to know about different sensors like Thermal sensors, Magnetic sensors, to know about Smart Sensors, Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface and the Automation

Module -I: Sensors / Transducers [8 Periods]

Principles – Classification – Parameters – Characteristics – Environmental Parameters (EP) – Characterization.

Mechanical and electromechanical sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors: – Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors

Module -II: Thermal Sensors [10 Periods]

Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermo sensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermo emf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors

Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors –Anisotropic Magneto resistive Sensing – Semiconductor Magneto resistors– Hall Effect and Sensors –Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros –Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flow meter – Switching Magnetic Sensors SQUID Sensors

Module -III: Radiation and Electro Analytical Sensors [9 Periods]

Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors.

Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

Module -IV: Smart Sensors and Applications [9 Periods]

Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation.

Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring

Module -V: Actuators **[10 Periods]**

Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches
Solenoids – D.C. Motors – A.C. motors – Stepper motors

TEXT BOOKS:

1. D. Patranabis , **Sensors and Transducers,**PHI Learning Private Limited.
2. W. Bolton ,**Mechatronics,**Pearson Education Limited.

REFERENCE BOOKS:

1. D. Patranabis **, Sensors and Actuators,** PHI, 2nd Ed, 2013.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Learn about sensor Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), and Characterization.
2. Know about different sensors like Thermal sensors, Magnetic sensors.
3. Know about Smart Sensors, Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface and the Automation

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Course Code: 54117 **Credits: 4**

M.Tech. – II Semester

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

(Professional Elective -IV)

PREREQUISITES: STLD and VLSI

OBJECTIVE: To understand the types of programmable logic devices and what are the differences between these devices. What are the different complex programmable logic devices with examples, to know the types of FPGA's and their programming technologies. What are the programmable logic block architectures, their interconnects and what are applications of FPGA's, to understand about the SRAM programmable FPGA's and their programming technology. What are examples of SRAM programmable FPGA's i.e Xilinx FPGA's with block diagrams.

Module - I: Introduction to Programmable Logic Devices [10 Periods]

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

Module –II: Field Programmable Gate Arrays [9 Periods]

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

Module – III : SRAM Programmable FPGSs [8 Periods]

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 andXC4000 Architectures.

Module -IV: Anti-Fuse Programmed FPGAs [8 Periods]

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

Module – V: Design Applications [9 Periods]

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Stephen M. Trimberger, Field **Programmable Gate Array Technology**,Springer International Edition.
2. Charles H. Roth Jr, Lizy Kurian John, **Digital Systems Design**, Cengage Learning.

REFERENCE BOOKS:

1. John V. Oldfield, Richard C. Dorf, **Field Programmable Gate Arrays**, Wiley India.
2. Pak K. Chan/Samiha Mourad, **Digital Design Using Field Programmable Gate Arrays**, Pearson Low Price Edition.
3. Ian Grout, Elsevier, **Digital Systems Design with FPGAs and CPLDs**, Newnes.
4. Wayne Wolf, **FPGA based System Design**, Prentice Hall Modern Semiconductor Design Series.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. The students will have the knowledge of types of programmable logic devices and what are the differences between these devices.
2. The students will have the knowledge of types of FPGA's and their programming technologies, programmable logic block architectures, their interconnects and what are applications of FPGA's.
3. The students will be able to know the programming technology of SRAM programmable FPGA's with their internal logic diagrams.

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Course Code: 54308 **Credits: 4**

M.Tech. – II Semester
WIRELESS COMMUNICATIONS AND NETWORKS
(Professional Elective -IV)

PREREQUISITES: Communication and Networks.

OBJECTIVE: To provide the students with the fundamental treatment about many practical and theoretical concepts that forms basic of wireless communications. To equip the students with various kinds of wireless networks and its operations. To prepare students to understand the concept of frequency reuse, and be able to apply it in the design of mobile cellular system. To train students to understand the architecture and operation of various wireless wide area networks such as GSM, IS-95, GPRS and SMSgt prepare students to understand the emerging technique OFDM and its importance in the wireless communications.

MODULE –I: INTRODUCTION TO WIRELESS COMMUNICATION SYSTEMS **[8 Periods]**

Evolution of mobile radio communications, examples of wireless communication systems- paging systems, cordless telephone systems, cellular telephone systems, comparison of common wireless communication systems, trends in cellular radio and personal communications.

Modern wireless communication systems: Second generation (2G) cellular networks, third generation (3G) wireless networks, wireless local loop (WLL) and LMDS, wireless local area networks (WLANs), Bluetooth and personal area networks (PANs).

MODULE - II: Mobile Radio Propagation: Large-Scale Path Loss [10 Periods]

Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models- Longley-Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

MODULE-III: Mobile Radio Propagation: Small –Scale Fading and Multipath **[10 Periods]**

Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading

effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

MODULE –IV: **[8 Periods]**

WI-FI AND THE IEEE 802.11 WIRELESS LAN STANDARD: IEEE 802 Architecture, IEEE 802.11 Architecture and Services, 802.11Medium Access Control, 802.11 Physical Layer, Other IEEE 802.11 Standards, Wi-Fi Protected Access.

BLUETOOTH AND IEEE 802.15: Overview, radio specification, baseband specification, link manager specification, logical link control and adaptation protocol, IEEE 802.15.

MODULE –V: **[8 Periods]**

MOBILE DATA NETWORKS: Introduction, data oriented CDPD network, GPRS and higher data rates, short messaging service in GSM, mobile application protocols.

WIRELESS ATM & HIPERLAN: Introduction, Wireless ATM, HIPERLAN, HIPERLAN-2.

TEXT BOOKS:

1. Theodore S. Rappaport, **Wireless Communications - Principles Practice**, Prentice Hall of India,New Delhi, 2nd edition , 2002.
2. William Stallings,**Wireless Communications and Networks**, Pearson Education,India, 2nd edition, 2009.
3. KavehPahLaven, Prashanth Krishna Murthy,**Principles of Wireless Networks - A Unified Approach**, Pearson Education, India, 2007.

REFERENCE BOOKS:

1. Dr. KamiloFeher, Wireless Digital Communications, Prentice Hall of India, New Delhi, 2003.
2. Jochen Schiller, Mobile Communications ,Pearson Education, India, 2nd edition, 2009.
3. Andreas F. Molisch, Wireless Communications, Wiley – India, New Delhi, 2006.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Understand the principles of wireless communications.
2. Understand fundamentals of wireless networking
3. Understand cellular system design concepts.
4. Analyze various multiple access schemes used in wireless communication.
5. Understand wireless wide area networks and their performance analysis.
6. Demonstrate wireless local area networks and their specifications.
7. Familiar with some of the existing and emerging wireless standards.
8. Understand the concept of orthogonal frequency division multiplexing.

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Course Code: 54119 **Credits: 4**

M.Tech. – II Semester

SYSTEM ON CHIP ARCHITECTURE

(Professional Elective -IV)

PREREQUISITES: Computer Architecture, Digital circuits and Embedded Systems.

OBJECTIVE: This course introduce to computer system design, with emphasis on fundamental ideas and analytical techniques that are applicable to a range of applications and architectures. This course introduces hardware and software programmability verses performance. This course introduces of entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices.

Module – I: Introduction to The System Approach [08 Periods]

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, an approach for SOC Design, System Architecture and Complexity.

Module – II: Processors [12 Periods]

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Module – III: Memory Design for Soc [10 Periods]

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

Module – IV: Interconnects Customization and Configuration [12 Periods]

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

Module – V: APPLICATION STUDIES / CASE STUDIES [08 Periods]

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, **"Computer System Design System on Chip"**, Wiely India Pvt. Ltd., 2012. (Modules I, II, III, IV & V)

REFERENCE BOOKS:

1. Steve Furber**, "ARM System on Chip Architecture",** Addison Wesley Professional, 2nd Edition, 2000.
2. Ricardo Reis, **"Design of System on a Chip: Devices and Components"**, Springer, 1st Edition, 2004.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Know how the system forms with the lot of component and has majority about system level interconnections
2. Understand hardware and software programmability verses performance
3. Know about entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices

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Course Code: 54309 **Credits: 4**

M.Tech. – II Semester

MULTI MEDIA AND SIGNAL CODING

(Professional Elective -V)

PREREQUISITES: Encoding and Decoding of Binary Data and also need concepts of Image, Audio and Video Processing.

OBJECTIVE: To learn about Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats, to know about Lossless compression algorithms like Run Length Coding, Variable Length Coding, Arithmetic Coding and Lossless JPEG image Compression, to learn about Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

Module - I: Introduction **[10 Periods]**

Multimedia: Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.
Color In Image And Video: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

Module - II: Video and Audio Concepts **[8 Periods]**
Video Concepts: Types of Video Signals, Analog Video, Digital Video.
Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

Module - III: Compression Algorithms **[9 Periods]**
Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.
Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet BasedCoding.
Image Compression Standards: JPEG and JPEG2000.

Module - IV: Video Compression Techniques **[10 Periods]**
Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding,Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

Module - V: Audio Compression Techniques **[9 Periods]**
ADPCM in Speech Coding, G.726 ADPCM, Vocoders – Phase Insensitivity, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

TEXT BOOKS:

1. Ze- Nian Li, Mark S. Drew, **Fundamentals of Multimedia,**PHI, 2010.
2.Mrinal Kr. Mandal , **Multimedia Signals & Systems**, Springer International Edition 1st Edition,2009.

REFERENCE BOOKS:

1. K.R. Rao, Zorans.Bojkoric, DragoradA.Milovanovic.**Multimedia Communication Systems-Techniques,Stds&Netwroks**, 1st Edition, 2002.
2. Ze- Nian Li, Mark S.Drew, **Fundamentals of Multimedia** , Pearson Education (LPE), 1st Edition,2009.
3. John F. KoegelBufond , **Multimedia Systems**, Pearson Education (LPE), 1st Edition, 2003.
4. A. Murat Tekalp, **Digital Video Processing,**PHI, 1996.
5.Yaowang, JornOstermann, Ya-QinZhang, **Video Processing and Communications**, Pearson, 2002.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Learn about Multimedia, World Wide Web, Overview of Multimedia Tools,Multimedia Authoring, Graphics/ Image Data Types, and File Formats.
2. Know about Lossless compression algorithms like Run Length Coding, Variable Length Coding, Arithmetic Coding and Lossless JPEG image Compression.
3. Learn about Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

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Course Code: 54118 **Credits: 4**

M.Tech. – II Semester

NETWORK SECURITY AND CRYPTOGRAPHY

(Professional Elective -V)

PREREQUISITES: Concepts of Security and Cryptography

OBJECTIVE: To learn about various security attacks, Conventional encryption methods. To learn about Public key cryptography and email privacy.

Module – I **[10 Periods]**

INTRODUCTION: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

Module - II **[10 Periods]**

MODERN TECHNIQUES: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random NumberGeneration.

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

Module - III **[8 Periods]**

NUMBER THEORY: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash Functions:

Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

Module – IV **[7 Periods]**

HASH AND MAC ALGORITHMS: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.

Digital signatures and Authentication Protocols: Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications: Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

Module - V **[10 Periods]**

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security: Web Security requirements, secure sockets layer and Transport layer security, Secure Electronic Transaction.

Intruders, Viruses and Worms: Intruders, Viruses and Related threats.

Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. William Stallings**, Cryptography and Network Security: Principles and Practice**, Pearson Education.
2. William Stallings, **Network Security Essentials (Applications and Standards)**, Pearson Education.

REFERENCE BOOKS:

1. Eric Maiwald , Fundamentals of Network Security, Dreamtech press
2. Charlie Kaufman, Radia Perlman and Mike Speciner **, Network Security - Private Communication in a Public World** , Pearson/PHI.
3. Whitman, Thomson , **Principles of Information Security**.
4. Robert Bragg, Mark Rhodes **, Network Security: The complete reference** ,TMH
5. Buchmann , **Introduction to Cryptography**, Springer.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Know about Attacks, Services and Mechanisms, Security attacks, Security services, Conventional Encryption model, Steganography, Classical Encryption Techniques.
2. Know about the Algorithms like Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.
3. Learn about Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, testing for primality, Euclid's Algorithm, the Chinese remainder theorem, and discrete logarithms.

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Course Code: 54104 **Credits: 4**

M.Tech. – II Semester

HARDWARE AND SOFTWARE CO-DESIGN

(Professional Elective - V)

PREREQUISITES: Concepts of Models and Architectures

OBJECTIVE: To design mixed hardware-software systems and the design of hardware-software interfaces, To focus on common underlying modeling concepts, and the trade-offs between hardware and software components, To learn about System –level specification, design representation for system level synthesis, system level specification languages.

Module –I: Co- Design Issues [10 Periods]

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- synthesis algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co synthesis.

Module –II: Prototyping and Emulation [8 Periods]

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Module –III: Compilation Techniques and Tools for Embedded Processor Architectures [8 Periods]

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Module –IV: Design Specification and Verification [10 Periods]

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Module –V: Languages For System – Level Specification And Design-I [9 Periods]

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for system – level specification and design-ii: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycossystem.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, **Hardware / Software Co- Design Principles and Practice**, Springer, 2009.

2. Giovanni De Micheli, Mariagiovanna Sami, **Hardware / Software Co- Design** ,KluwerAcademic Publishers,2002.

REFERENCE BOOKS:

1. Patrick R. Schaumont , **A Practical Introduction to Hardware/Software Co-design**, Springer,2010.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Able to design mixed hardware-software systems and the design of hardware-software interfaces
2. Able to focus on common underlying modeling concepts, , and the trade-offs between hardware and software components.
3. Able to learn about System –level specification, design representation for system level synthesis, system level specification languages.

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Course Code: 54125 **Credits: 4**

M.Tech. – II Semester

SCRIPTING LANGUAGES

(Professional Elective -VI)

PREREQUISITES: Computer Languages.

OBJECTIVE: To learn about Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data and working with arrays , To learn about The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes , To learn about Objects, Classes, Encapsulation, Data Hierarchy.

Module - I: INTRODUCTION **[8 Periods]**

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

Module - II: ADVANCED PERL **[8 Periods]**

Finger points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

Module - III: TCL **[7 Periods]**

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

Module - IV: ADVANCED TCL **[9 Periods]**

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

Module - V: TK AND JAVASCRIPT **[10 Periods]**

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.Java Script – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation,Data Hierarchy.

TEXT BOOKS:

1. David Barron**,The World of Scripting Languages,** Wiley Student Edition, 2010.
2. Ken Jones and Jeff Hobbs.**Practical Programming in Tcl and Tk - Brent Welch**,Fourth edition.
3. Herbert Schildt, **Java the Complete Reference ,** TMH,7th Edition.

REFERENCE BOOKS:

1. ClifFlynt, TCL/**TK: A Developer's Guide ,**Morgan Kaufmann SerieS , 2003.
2. **Tcl and the TK Toolkit- John Ousterhout**, Kindel Edition , 2nd Edition, 2009.
3. WojciechKocjan and PiotrBeltowski,**Tcl 8.5 Network Programming book,** Packt Publishing.
4. Bert Wheeler, **Tcl/Tk 8.5 Programming Cookbook.**

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Learn about Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data and working with arrays.
2. Learn about The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow,Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes.
3. Learn about Objects, Classes, Encapsulation, Data Hierarchy.

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Course Code: 54124 **Credits: 4**

M.Tech. – II Semester

AD HOC WIRELESS NETWORKS

(Professional Elective -VI)

PREREQUISITES: Wireless Networks and Protocols

OBJECTIVE: To learn about Introduction, Fundamentals of WLANS,IEEE802.11 Standard, HIPERLAN Standard, Bluetooth and Home RF, To learn about Issues in Ad Hoc Wireless Networks, AD Hoc Wireless Internet.MAC Protocols for Ad Hoc Wireless Networks and Issues in designing a MAC protocol for Ad Hoc Wireless network, To learn about issues in designing a routing protocol for ad hoc wireless networks, classification of routing protocols,tabel-driven routing protocols on-demand routing protocols, hybrid routing protocols,routing protocols with efficient flooding mechanism, hierarchical; routing protocols, power-aware routing protocols.

Module – I : WIRELESS LANS AND PANS [8 Periods]

Introduction, Fundamentals of WLANS, IEEE802.11 Standard. HIPERLAN Standard, Bluetooth, Home RF. Wireless Internet: Wireless internet, mobile IP, TCP in Wireless Domain, WAP, Optimizing Web over Wireless.

Module – II : Adhoc wireless networks [10 Periods]

Introduction, Issues in Ad Hoc Wireless Networks, AD Hoc Wireless Internet.MAC Protocols for Ad Hoc Wireless Networks: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless network, Design goals of MAC Protocol, contention - Based Protocols, contention -based protocol with Reservation Mechanism, contention - Based MAC Protocols with Scheduling Mechanisms, MAC protocol that use Directional Antenna, other MAC Protocol

Module – III: PROTOCOLS [10 Periods]

Routing: Introduction issues in designing a routing protocol for ad hoc wireless networks, classification of routing protocols, table-driven routing protocols, on-demand routing protocols, hybrid routing protocols, routing protocols with efficient flooding mechanism, hierarchical; routing protocols, power-aware routing protocols.

Transport layer and security protocols: introduction, issues in designing a transport layer protocol for ad hoc wireless networks, design goals of a transport layer protocol for ad hoc wireless networks, classification of transport layer solutions, TCP over ad hoc wireless networks, other transport layer protocol fpr ad hoc wireless networks, security provisioning, network security attacks, key management, secure routing in ad hoc wireless networks

Module - IV: QUALITY OF SERVICE [9 Periods]

Introduction, issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions, MAC Layer solutions, Network layer solutions, QoS Frame Works for Ad Hoc Wireless Network**.**

Energy management: Introduction, Need for Energy Management in Ad Hoc Wireless Networks, Classification of Ad Hoc Wireless networks, Battery Management Schemes, Transmission Power Management Schemes, System power management schemes.

Module - V: WIRELESS SENSOR NETWORKS [8 Periods]

Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocol for Sensor Networks, Location Discovery, Quality of Sensor Networks, Evolving Standards, Other Issues.

TEXT BOOKS:

1. C.Siva Ram Murthy and B.S.Manoj, **Ad HOC Wireless Networks:Architectures and protocols,** PHI,2004.
2. JagannathamSarangapani, Wireless **Ad-Hoc and Sensor Networks: Protocols, Performance and control** –CRC Press

REFERENCE BOOKS:

1. C.K.Toh,**Ad -Hoc Mobile Wireless Networks: Protocols And Systems,** Pearson Education,1ed.
2. C.S. Raghavendra, Krishna M.Sivalingam, **Wireless Sensor Networks,** 2004, Springer

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Learn about Introduction, Fundamentals of WLANS, IEEE802.11 Standard, HIPERLAN Standard, Bluetooth and Home RF.
2. Learn about Issues in Ad Hoc Wireless Networks, AD Hoc Wireless Internet.MAC Protocols for Ad Hoc Wireless Networks and Issues in designing a MAC protocol for Ad Hoc Wireless network.
3. Learn about issues in designing a routing protocol for ad hoc wireless networks, classification of routing protocols, table-driven routing protocols, on-demand routing protocols, hybrid routing protocols, routing protocols with efficient flooding mechanism, hierarchical; routing protocols, power-aware routing protocols.

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Course Code: 54122 **Credits: 4**

M.Tech. – II Semester

DEVICE MODELLING

(Professional Elective – VI)

PREREQUISITES: Engineering Physics and Semiconductor Physics

OBJECTIVE: To know about Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation , To learn about Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model dynamic model, Parasitic effects – SPICE model –Parameter extraction , To learn about An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS

Module - I: **[8 Periods]**

INTRODUCTION TO SEMICONDUCTOR PHYSICS: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

Module -II: **[9 Periods]**

INTEGRATED DIODES: Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models
Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model dynamic model, Parasitic effects – SPICE model –Parameter extraction.

Module - III: **[11 Periods]**

INTEGRATED MOS TRANSISTOR:NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics– MOS FET SPICE model level 1, 2, 3 and 4.

Module - IV: **[10 Periods]**

VLSI FABRICATION TECHNIQUES: An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements –Interconnects circuit elements

Module - V: **[8 Periods]**

MODELING OF HETERO JUNCTION DEVICES: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

1. Tyagi M. S, **Introduction to Semiconductor Materials and Devices,** John Wiley Student Edition,2008.
2. Ben G. Streetman, **Solid State Circuits**, Prentice Hall, 1997

REFERENCE BOOKS:

1. Sze S. M, **Physics of Semiconductor Devices**, Mcgraw Hill ,2nd Edition, New York, 1981.
2. Tor A. Fijedly, **Introduction to Device Modeling and Circuit Simulation** ,Wiley-Interscience, 1997.
3. Ming-BO Lin, **Introduction to VLSI Systems: A Logic, Circuit and System Perspective ,** CRC Press, 2011

COURSE OUTCOMES:

1. Able to know about Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
2. Able to learn about Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model dynamic model, Parasitic effects – SPICE model –Parameter extraction.
3. Able to learn about An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS

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Course Code: 54310 **Credits: 2**

M.Tech. – II Semester

ADVANCED EMBEDDED SYSTEM LAB

Note: The following programs are to be implement on ARM based Processors using Keil IDE and Flash magic.

List of experiments:

1. Introduction to ARM Development Board & Software
2. Simple Assembly Program for
    a. Addition | Subtraction | Multiplication | Division
3. Simple Assembly Program for
    a. Operating Modes, System Calls and Interrupts
    b. Loops, Branches
4. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
5. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
6. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
7. Program to demonstrates a simple interrupt handler and setting up a timer
8. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
9. Program to Interface 8 Bit LED and Switch Interface
10. Program to implement Buzzer Interface on IDE environment
11. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
12. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.

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Course Code: 54311 **Credits: 2**

M.Tech. – II Semester
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Course Code: 54312 **Credits: 4**

M.Tech. – III Semester
Comprehensive Viva - voce

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Course Code: 54313 **Credits: 8**

M.Tech. – III Semester
Project Work Part I

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Course Code: 54314 **Credits: 8**

M.Tech. – IV Semester
Project Work Part II

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Course Code: 54315 **Credits: 12**

M.Tech. – IV Semester
Project Viva – Voce